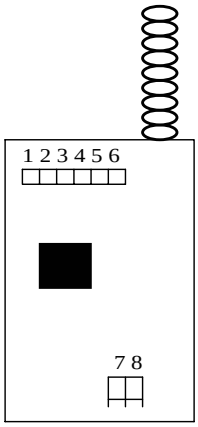
FSK TRANSCEIVER MODULE

Description

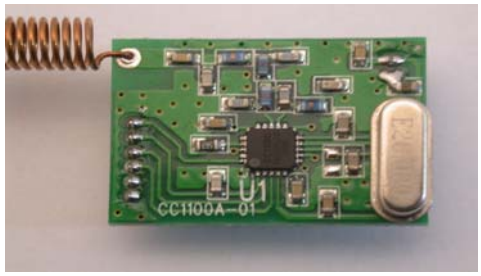
ST-TR1100 is an FSK Transceiver module, which is designed by the Chipcon IC(CC1100). The ST-TR1100 is a true single-chip UHF transceiver, It base on 3 wire digital serial interface and an entire Phase-Locked Loop (PLL) for precise local oscillator generation .so the frequency could be setting. It can use in UART / NRZ / Manchester encoding / decoding. ST-TR1100 owns a high performance and low cost. It could easily to design your product.

It can be used on wireless security system or specific remote-control function and others wireless system



Features

- Low power consumption.
- Integrated bit synchronizer.
- Integrated IF and data filters.
- High sensitivity (type -108dBm at 1.2kbps)
- Programmable output power -20dBm~9dBm
- Operation temperature range : -40℃～＋85℃
- Operation voltage: 1.8~3.6 Volts.
- Available frequency at : 423~443 MHz
- Digital RSSI
- Digital function for package format



Applications

- Car security system
- Remote keyless entry
- Garage door controller
- Home security
- Wireless mouse
- Automation system

Pin1: CSN

Pin2: GDO0

Pin3: GDO2

Pin4: SO

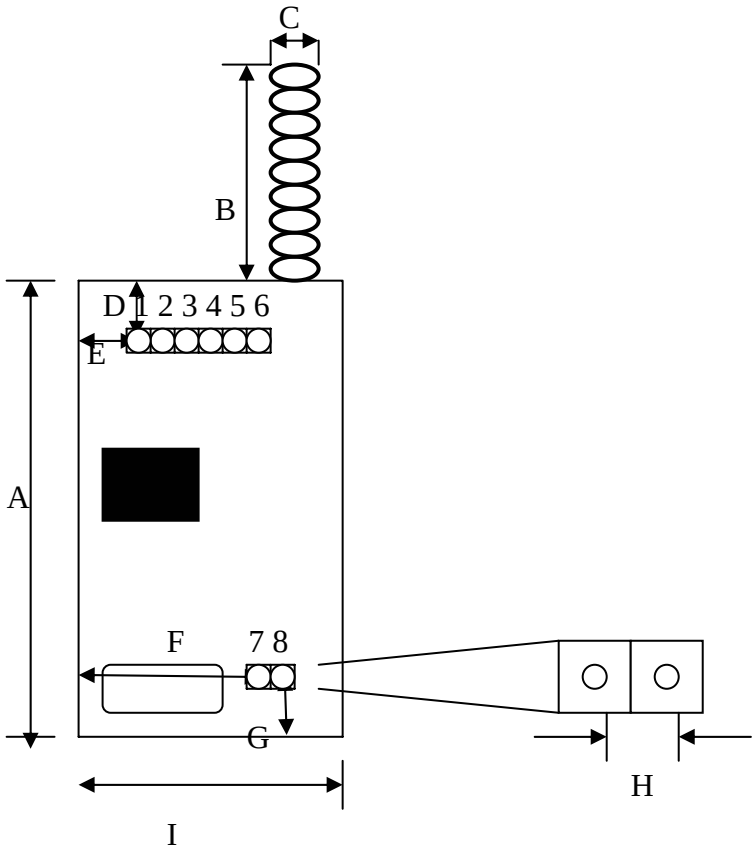
Pin5: SCLK

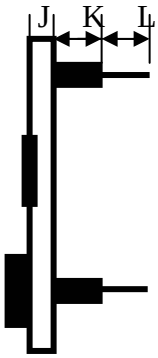
Pin6: SI

Pin7: GND

Pin8: VCC

Pin Dimension





A	23.4mm	F	13.1mm	K	2.17mm
B	20mm	G	2.6mm	L	3.6mm
C	4.55mm	H	1.27mm	Pin	0.5mm
D	1.8mm	I	16.3mm		
E	2.4mm	J	1 mm		

PIN#	Pin name	Pin type	Description
1	CSN	Digital input	Serial configuration interface ,chip select
2	GDO0	Digital I/O	Digital output pin for general use: >Test signals >FIFO status signals >Clear Channel indicator >Clock output RX data >Serial output RX data >Serial input TX data Also used as analog test I/O for prototype/production testing
3	GDO2	Digital I/O	Digital output pin for general use >Test signals >FIFO status signals >Clear Channel indicator >Clock output,down-divided from Xosc >Serial output RX data
4	SO	Digital Output	Serial configuration interface, clock input Optional general output pin when CSN is hight
5	SCLK	Digital input	Serial configuration interface, clock input
6	SI	Digital input	Serial configuration interface, data input
7	GND	Ground	GND
8	VCC	Power	1.8~3.6V power supply

3 Electrical Specifications

Tc = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's CC1100EM reference design.

Parameter	Min	Typ	Max	Unit	Condition
Current consumption in power down modes		900		nA	Voltage regulator to digital part off, register values retained, low-power RC oscillator running (SLEEP state with WOR enabled)
		400		nA	Voltage regulator to digital part off, register values retained (SLEEP state)
		90		µA	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with MCSM0.OSC_FORCE_ON set)
		160		µA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
Current consumption		15		µA	Automatic RX polling once each second, using low-power RC oscillator, with 460kHz filter bandwidth and 250kbps data rate, PLL calibration every 4th wakeup. Average current with signal in channel *below* carrier sense level.
		34		µA	Same as above, but with signal in channel *above* carrier sense level, 1.9ms RX timeout, and no preamble/sync word found.
		1.8		µA	Automatic RX polling every 15th second, using low-power RC oscillator, with 460kHz filter bandwidth and 250kbps data rate, PLL calibration every 4th wakeup. Average current with signal in channel below carrier sense level.
		15		µA	Same as above, but with signal in channel *above* carrier sense level, 14ms RX timeout, and no preamble/sync word found.
		1.9		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		8.7		mA	Only the frequency synthesizer running (after going from IDLE until reaching RX or TX states, and frequency calibration states)
Current consumption, 315MHz		26.9		mA	Transmit mode, +10dBm output power
		18.3			Transmit mode, 5dBm output power
		15.1			Transmit mode, 0dBm output power
		13.4			Transmit mode, –10dBm output power
		15.1			Receive mode, 2.4kbps, input at sensitivity limit
		14.0			Receive mode, 2.4kbps, input 30dB above sensitivity limit
		16.2			Receive mode, 250kbps, input at sensitivity limit
		15.1			Receive mode, 250kbps, input 30dB above sensitivity limit
Current consumption, 433MHz		28.8		mA	Transmit mode, +10dBm output power
		19.3			Transmit mode, 5dBm output power
		16.1			Transmit mode, 0dBm output power
		14.3			Transmit mode, –10dBm output power
		15.6			Receive mode, 2.4kbps, input at sensitivity limit
		14.5			Receive mode, 2.4kbps, input 30dB above sensitivity limit
		16.5			Receive mode, 250kbps, input at sensitivity limit
		15.5			Receive mode, 250kbps, input 30dB above sensitivity limit

Parameter	Min	Typ	Max	Unit	Condition
Current consumption, 868/915MHz		30.3		mA	Transmit mode, +10dBm output power
		19.7			Transmit mode, 5dBm output power
		16.6			Transmit mode, 0dBm output power
		14.0			Transmit mode, –10dBm output power
		15.4			Receive mode, 2.4kbps, input at sensitivity limit
		14.2			Receive mode, 2.4kbps, input 30dB above sensitivity limit
		16.2			Receive mode, 250kbps, input at sensitivity limit
		15.2			Receive mode, 250kbps, input 30dB above sensitivity limit

Table 3: Electrical Specifications

4 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency range	300		348	MHz	
	400		464	MHz	
	800		928	MHz	
Data rate	1.2		500	kbps	Modulation formats supported: (Shaped) MSK (also known as differential offset QPSK) up to 500kbps 2-FSK up to 500kbps GFSK and OOK/ASK (up to 250kbps) Optional Manchester encoding (halves the data rate).

Table 4: General Characteristics

5 RF Receive Section

Tc = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's CC1100EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential input impedance		TBD		Ω	Follow CC1100EM reference design
Receiver sensitivity 315/433/868/915MHz		–110		dBm	2-FSK, 1.2kbps, 5.2kHz deviation, 1% packet error rate, 62 bytes packet length, 58kHz digital channel filter bandwidth
		–100		dBm	2-FSK, 38.4kbps, 20kHz deviation, 1% packet error rate, 62 bytes packet length, 100kHz digital channel filter bandwidth
		-88		dBm	2-FSK, 250kbps, 127kHz deviation, 1% packet error rate, 62 bytes packet length, 540kHz digital channel filter bandwidth
		-88		dBm	OOK, 250kbps OOK, 1% packet error rate, 62 bytes packet length, 540kHz digital channel filter bandwidth
Saturation		–15		dBm	
Digital channel filter bandwidth	58		650	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0MHz crystal).
Adjacent channel rejection, 868MHz		23		dB	2-FSK, 38.4kbps, 20kHz deviation, 1% packet error rate, 62 bytes packet length, 100kHz digital channel filter, 150kHz channel spacing Desired channel 3dB above the sensitivity limit.
Alternate channel rejection, 868MHz		33		dB	2-FSK, 38.4kbps, 20kHz deviation, 1% packet error rate, 62 bytes packet length, 100kHz digital channel filter, 150kHz channel spacing Desired channel 3dB above the sensitivity limit.
Image channel rejection, 868MHz		29		dB	2-FSK, 38.4kbps, 20kHz deviation, 1% packet error rate, 62 bytes packet length, 100kHz digital channel filter, 150kHz channel spacing, IF frequency 305kHz Desired channel 3dB above the sensitivity limit.
Blocking at 1MHz offset, 868MHz		52		dB	Desired channel 3dB above the sensitivity limit. Compliant to ETSI EN 300 220 class 2 receiver requirement.
Blocking at 2MHz offset, 868MHz		54		dB	Desired channel 3dB above the sensitivity limit. Compliant to ETSI EN 300 220 class 2 receiver requirement.
Blocking at 5MHz offset, 868MHz		61		dB	Desired channel 3dB above the sensitivity limit. Compliant to ETSI EN 300 220 class 2 receiver requirement.
Blocking at 10MHz offset, 868MHz		64		dB	Desired channel 3dB above the sensitivity limit. Compliant to ETSI EN 300 220 class 2 receiver requirement.
Spurious emissions			–57 –47	dBm dBm	25MHz – 1GHz Above 1GHz

Table 5: RF Receive Section

6 RF Transmit Section

Tc = 25°C, VDD = 3.0V, +10dBm if nothing else stated. Measured on Chipcon's CC1100EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance		TBD		Ω	Follow CC1100EM reference design
Output power, highest setting		10		dBm	Output power is programmable, and full range is available in all frequency bands. Delivered to a 50Ω single-ended load via Chipcon reference RF matching network.
Output power, lowest setting		–30		dBm	Output power is programmable, and full range is available in all frequency bands. Delivered to a 50Ω single-ended load via Chipcon reference RF matching network.
Spurious emissions and harmonics, 433/868MHz			–36 –54 –47 –30	dBm dBm dBm dBm	25MHz – 1GHz 47-74, 87.5-118, 174-230, 470-862MHz 1800MHz-1900MHz (restricted band in Europe), when the operating frequency is below 900MHz (2^{nd} harmonic can not fall within this band when used in Europe) Otherwise above 1GHz
Spurious emissions, 315/915MHz			-49.2 -41.2	dBm EIRP dBm EIRP	<200µV/m at 3m below 960MHz. <500µV/m at 3m above 960MHz.
Harmonics 315MHz			-20 -41.2	dBc dBm	2^{nd}, 3^{rd} and 4^{th} harmonic when the output power is maximum 6mV/m at 3m. (-19.6dBm EIRP) 5^{th} harmonic
Harmonics 915MHz			-20 -41.2	dBc dBm	2^{nd} harmonic 3^{rd}, 4^{th} and 5^{th} harmonic

Table 6: RF Transmit Parameters

Mark:

1. About Detail Specifications , Pls see CC1100 Data sheet .
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